

March 1997

Features

- **Static CMOS Silicon-On-Sapphire Circuitry CD4000-Series Compatible**
- **Compatible with CDP1800-Series Microprocessors at Maximum Speed**
- **Fast Access Time. 100ns Typ. at $V_{DD} = 5V$**
- **Single Voltage Supply**
- **No Precharge or External Clocks Required**
- **Low Quiescent and Operating Power**
- **Separate Data Inputs and Outputs**
- **High Noise Immunity 30% of V_{DD}**
- **Memory Retention for Standby Battery Voltage Down to 2V at +25°C**
- **Latch-Up-Free Transient-Radiation Tolerance**

Description

The CDP1821C/3 is a 1024-word x 1-bit CMOS silicon-on-sapphire (SOS), fully static, random-access memory designed for use in CDP1800 microprocessor systems. This device has a recommended operating voltage range of 4V to 6.5V.

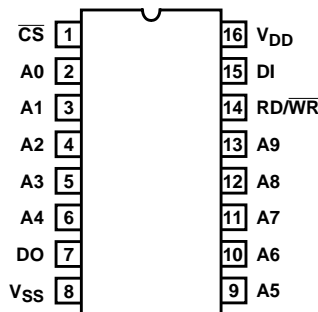
The output state of the CDP1821C/3 is a function of the input address and chip-select states only. Valid data will appear at the output in one access time following the latest address change to a selected chip. After valid data appears, the address may be changed immediately. It is not necessary to clock the chip-select input or any other input terminal for fully static operation; therefore the chip-select input may be used as an additional address input. When the device is in an unselected state ($\overline{CS} = 1$), the internal write circuitry and output sense amplifier are disabled. This feature allows the three-state data outputs from many arrays to be OR-tied to a common bus for easy memory expansion.

Ordering Information

PACKAGE	TEMP. RANGE	PART NUMBER	PKG. NO.
SBDIP	-55°C to +125°C	CDP1821CD3	D16.3

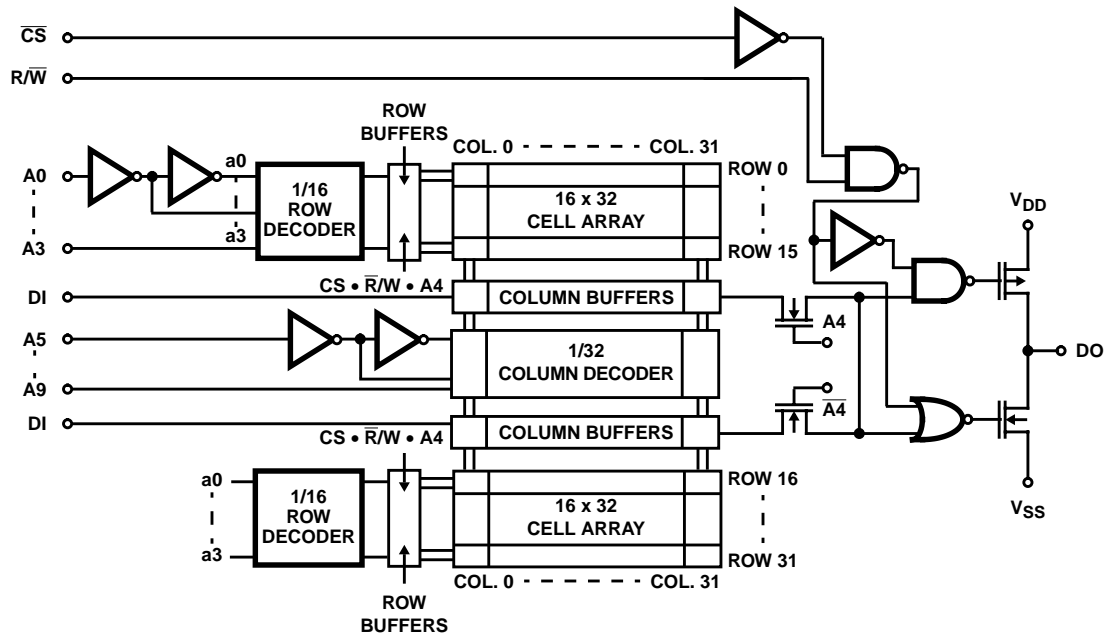
Pinout

**CDP1821C/3
(SBDIP)
TOP VIEW**



CDP1821C/3

Functional Block Diagram



OPERATIONAL MODES

MODE	INPUTS		OUTPUT
	READ/WRITE R/W	CHIP-SELECT CS	DATA OUTPUT DO
Standby	X	1	High Impedance
Write	0	0	High Impedance
Read	1	0	Contents of Addressed Call

X = Don't Care Logic 1 = High Logic 0 = Low

CDP1821C/3

Absolute Maximum Ratings

DC Supply Voltage Range, (V_{DD})
 (All Voltages Referenced to V_{SS} Terminal) -0.5V to +7V
 Input Voltage Range, All Inputs -0.5V to $V_{DD} + 0.5V$
 DC Input Current, Any One Input. $\pm 10mA$

Thermal Information

Thermal Resistance (Typical) θ_{JA} ($^{\circ}C/W$) θ_{JC} ($^{\circ}C/W$)
 SBDIP Package 75 20
 Maximum Operating Temperature Range (T_A) -55 $^{\circ}C$ to +125 $^{\circ}C$
 Maximum Storage Temperature Range (T_{STG}) . . . -65 $^{\circ}C$ to +150 $^{\circ}C$
 Maximum Lead Temperature (During Soldering) +265 $^{\circ}C$
 Maximum Junction Temperature +150 $^{\circ}C$

Recommended Operating Conditions T_A = Full Package-Temperature Range. For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges:

PARAMETER	CDP1821CD/3		UNITS
	MIN	MAX	
DC Operating Voltage Range	4	6.5	V
Input Voltage Range	V_{SS}	V_{DD}	V

Static Electrical Specifications $V_{DD} = 5V \pm 5\%$

PARAMETER	SYMBOL	CONDITIONS	-55 $^{\circ}C$, +25 $^{\circ}C$		+125 $^{\circ}C$		UNITS
			MIN	MAX	MIN	MAX	
Quiescent Device Current (Note 1)	I_{DD}	$V_{IN} = 0V$ or V_{DD}	-	260	-	1000	μA
Output Low Drive (Sink) Current (Note 1)	I_{OL}	$V_{OUT} = 0.4V$	2.7	-	1.6	-	mA
Output High Drive (Source) Current (Note 1)	I_{OH}	$V_{OUT} = V_{DD} - 0.4V$	-1.3	-	-0.8	-	mA
Output Voltage Low-Level	V_{OL}	-	-	0.1	-	0.5	V
Output Voltage High-Level	V_{OH}	-	$V_{DD} - 0.1$	-	$V_{DD} - 0.5$	-	V
Input Low Voltage	V_{IL}	-	-	$0.3 V_{DD}$	-	$0.3 V_{DD}$	V
Input High Voltage	V_{IH}	-	$0.7 V_{DD}$	-	$0.7 V_{DD}$	-	V
Input Current (Note 1)	I_{IN}	$V_{IN} = 0V$ or V_{DD}	-	2.6	-	10	μA
Three-State Output Leakage Current (Note 1)	I_{OUT}	$V_{IN} = 0V$ or V_{DD}	-	2.6	-	10	μA
Operating Current (Note 2)	I_{DD1}	-	-	5	-	10	mA
Input Capacitance	C_{IN}	-	-	7.5	-	7.5	pF
Output Capacitance	C_{OUT}	-	-	15	-	15	pF

NOTES:

1. Limits designate 100% testing. All other limits are designer's parameters under given test conditions and do not represent 100% testing
2. Measured with 1 μs read-cycle time and outputs floating.

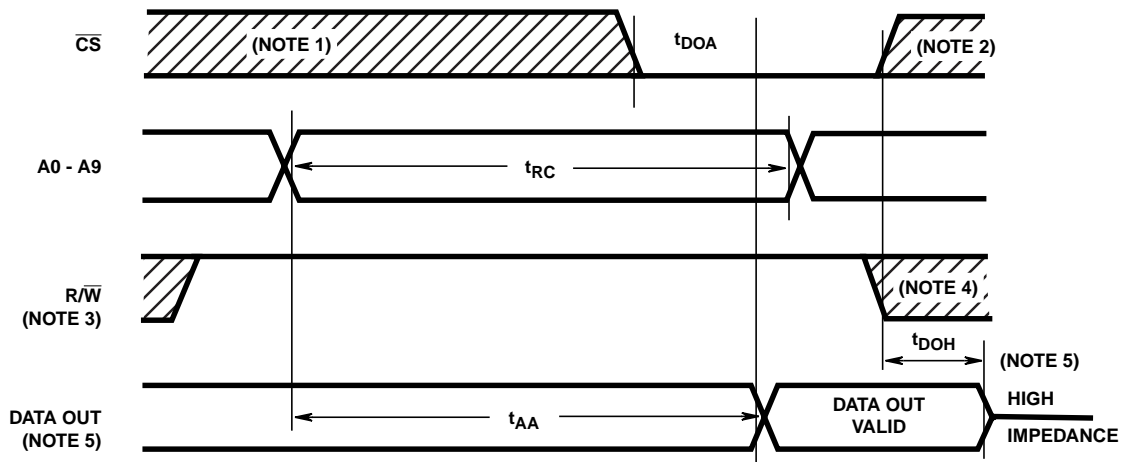
CDP1821C/3

Read Cycle Dynamic Electrical Specifications $t_R, t_F = 10\text{ns}, C_L = 50\text{pF}$

PARAMETER	SYMBOL	V_{DD} (V)	-55°C, +25°C		+125°C		UNITS
			MIN	MAX	MIN	MAX	
Data Access Time (Note 1)	t_{DA}	5	-	190	-	255	ns
Read Cycle Time	t_{RC}	5	190	-	255	-	ns
Output Enable Time	t_{EN}	5	65	-	90	-	ns
Output Disable Time	t_{DIS}	5	-	65	-	90	ns

NOTE:

1. 100% testing. All other limits are designer's parameters under given test conditions and do not represent 100% testing.



NOTES:

1. Chip-Select (\overline{CS}) permitted to change from high to low level or remain low on a selected device.
2. Chip-Select (\overline{CS}) permitted to change from low to high level or remain low.
3. Read/Write (R/\overline{W}) must be at a high level during all address transitions.
4. Don't care.
5. Data-Out (DO) is a high impedance within t_{DIS} ns after the falling edge of R/\overline{W} or the rising edge of \overline{CS} .

FIGURE 1. READ CYCLE TIMING DIAGRAM

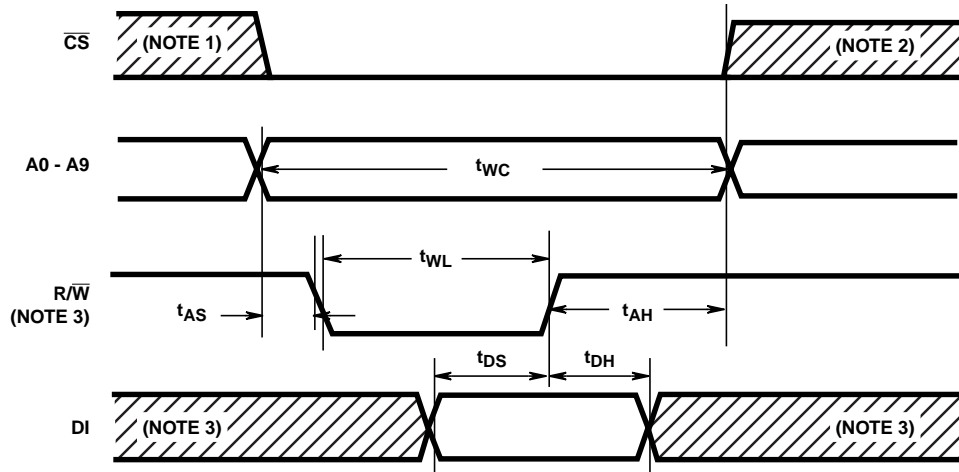
CDP1821C/3

Write Cycle Dynamic Electrical Specifications $t_R, t_F = 10\text{ns}, C_L = 50\text{pF}$

PARAMETER	SYMBOL	V_{DD} (V)	-55°C, +25°C		+125°C		UNITS
			MIN	MAX	MIN	MAX	
Write Cycle Time	t_{WC}	5	300	-	420	-	ns
Address Setup Time (Note 1)	t_{AS}	5	60	-	84	-	ns
Address Hold Time (Note 1)	t_{AH}	5	130	-	180	-	ns
Input Data Setup Time (Note 1)	t_{DS}	5	90	-	125	-	ns
Input Data Hold Time (Note 1)	t_{DH}	5	60	-	84	-	ns
Read/Write Pulse Width Low (Note 1)	t_{WL}	5	110	-	155	-	ns

NOTE:

1. 100% testing. All other limits are designer's parameters under given test conditions and do not represent 100% testing.



NOTES:

1. Chip-Select (\overline{CS}) permitted to change from high to low level or remain low on a selected device.
2. Chip-Select (\overline{CS}) permitted to change from low to high level or remain low.
3. Don't care.

FIGURE 2. WRITE CYCLE TIMING DIAGRAM

Data Retention Specifications

PARAMETER	SYMBOL	TEST CONDITIONS		-55°C, +25°C		+125°C		UNITS
		V _{DR} (V)	V _{DD} (V)	MIN	MAX	MIN	MAX	
Minimum Data Retention Voltage (Note 1)	V _{DD}	-	-	-	2	-	2.5	V
Data Retention Quiescent Current (Note 1)	I _{DD}	2	-	-	50	-	200	μA
Chip Deselect to Data Retention Time	t _{CDR}	-	5	450	-	650	-	ns
Recovery to Normal Operation Time	t _{RC}	-	5	450	-	650	-	ns

NOTE:

1. 100% testing. All other limits are designer's parameters under given test conditions and do not represent 100% testing

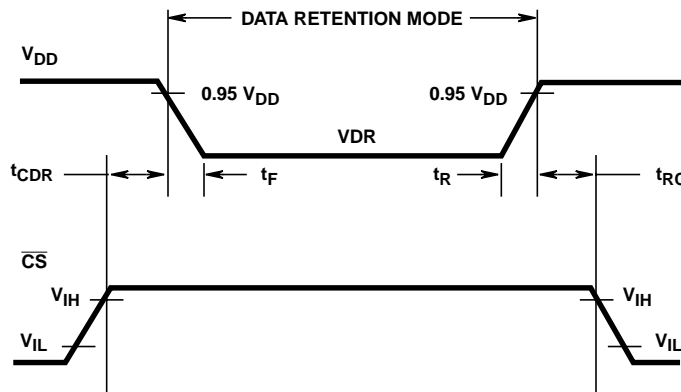
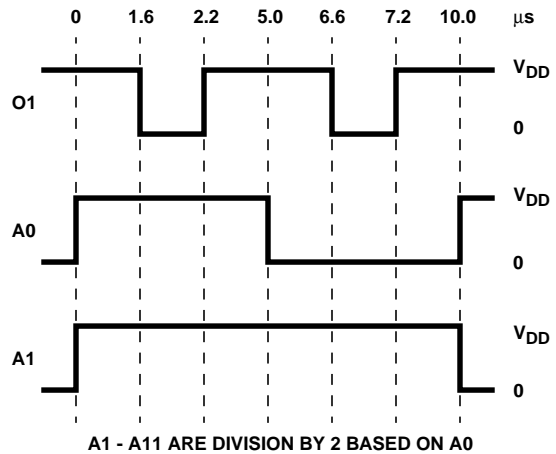
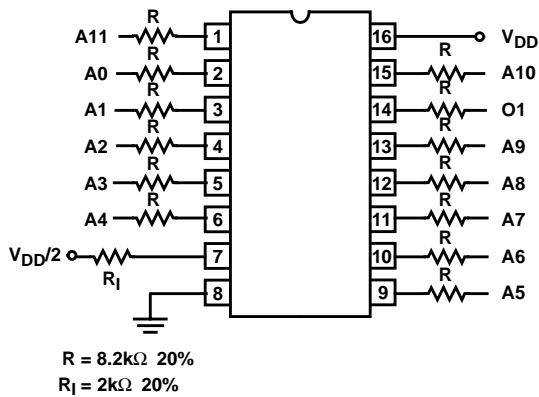


FIGURE 3. LOW V_{DD} DATA RETENTION WAVEFORMS AND TIMING DIAGRAM

Burn-In Circuit



PACKAGE	V _{DD}	TEMPERATURE	DURATION
D	7V	+125°C	160 Hrs.

FIGURE 4. DYNAMIC/OPERATING BURN-IN CIRCUIT AND TIMING DIAGRAM

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